Control of Reduced Switches Count and Classical Multilevel Inverters: a Comparison

Jorel Landry Owona^{1,3*}, Marie Danielle Fendji², Joseph Yves Effa³, and Eric Duckler Kenmoe Fankem³

¹National Committee for Development of Technologies, 1457 Yaounde Cameroon ²Faculty of Engineering and Technology, University of Buea, 63 Buea, Cameroon ³Faculty of Sciences, University of Ngaoundere, 454 Ngaoundere, Cameroon

Abstract. Multilevel inverter has appeared as one of the important topologies in the area of high power and medium voltage because it can efficiently realize lower harmonics with reduced switching frequency. These Multilevel inverters (MLI) improve the energy quality shaped by producing many voltage levels. However, improving the quality of the output voltage of a multilevel inverter requires many switches, which tend to weigh down the structure and make it complex to control. This work deals with a comparison in terms of the spectral content of two configurations of thirty-one-level inverters for injection into the electrical grid. The first configuration is a classical cascaded H-bridge and the second one is a reconfigured Packed U-Cell (PUC) multilevel inverter. The classical configuration requires sixteen switches while the second uses only ten ones. The control technique based on the half-height modulation was performed and the Total Harmonic Distortion (THD) is calculated for each topology. For the PUC, we got a THD equal to 2.61% while we got 2.72% for the cascaded H-bridge. These results obtained in the MATLAB/Simulink environment, show that the reconfigured structure of the PUC inverter is a good candidate for injection into the electrical network.

Keywords: Multilevel Inverters, Reduced switches, Half-height modulation, Total Harmonic Distortion

1 Introduction

The most important element of a photovoltaic solar system remains the inverter. Two configurations of such a system exist: the off-grid PV systems and gridconnected PV systems [1], [2]. The two-level inverter and conventional inverters are used in each of these configurations. However, the two-level inverter has several limitations such as the inability to withstand high dv/dt voltage stresses and the inability to produce voltages less polluted by harmonics. To improve the performance of this type of converter the power electronics thanks to its evolution proposes a new structure: the multilevel inverter. The first multilevel inverter was the multicell inverter that appears in 1975 [3] which later became the Cascaded H-bridge (CHB) inverter. Other topologies namely the neutral point clamped (NPC) [4] and Flying Capacitors (FC) inverters [5] were designed respectively in 1980 and 1992. The control of these converters is generally done by Pulse Width Modulation (PWM) which thus causes enormous losses because the power switches operate at a very high frequency. Among these classical multilevel inverters, the cascaded H-bridge inverter has a particular advantage that of using several continuous power sources while the others use only one. It is therefore necessary to multiply the number of diodes and capacitors in both of the topologies to be able to produce as many voltage levels as the cascade H-bridge inverter. The latter is therefore more recommended for photovoltaic systems. In the literature, two configurations of cascaded inverters are distinguished:

symmetric and asymmetric structures determined by the amplitude of the DC voltages. For a symmetric architecture, the amplitude of the continuous sources is identical. For an asymmetric architecture, the DC sources have different values [6], [7] to reach the maximum voltage. Moreover, producing a multilevel voltage with less THD requires several DC sources and several switches, which increases the complexity of the structure and the control. To resolve this problem, asymmetric inverters are used to reduce the number of components, power losses and increase efficiency in the case of the grid-connected photovoltaic (PV) systems. Despite the advantages mentioned above, the control of multilevel structures with reduced switches remains quite more complex than symmetric structures. The present work, deals with the control method of a classical asymmetric structure on the one hand and on the other of an asymmetric structure with reduced switches. In addition, a comparison based on the spectral content point of view is carried out under the MATLAB/Simulink platform.

2 Methodology

2.1 Cascaded H-bridge thirty-one-levels

The cascaded H-bridge was the first multilevel structure proposed by Baker and Bannister in [3]. This multilevel inverter is illustrated in Fig. 1. This basic structure consists of a DC power source and four switches. To produce thirty-one-levels, we put in series four Hbridges and we use an arrangement based on a geometric

^{*} Corresponding author: jorelowona@gmail.com

progression of 2^k (k=0,1, 2..., n) with the following ratio 1:2:4:8. The different values of DC sources of the thirtyone-levels cascaded H-bridge are Vdc, 2Vdc, 4Vdc and 8Vdc. The different possible output voltage levels are represented in Fig. 2. For producing all the voltage levels, the switching states of the upper switches are depicted in the Table 1.



Fig. 1. H-bridge three levels.

Table 1. Output voltage levels and switching states for
cascaded H-bridge inverter

VLoad	S1	S 3	S 5	S 7	S 9	S11	S13	S15
0	1	1	1	1	1	1	1	1
Vdc	1	1	1	1	1	1	1	0
2Vdc	1	1	1	0	1	0	1	1
3Vdc	1	1	1	1	1	0	1	1
4Vdc	1	1	1	0	1	1	1	1
5Vdc	1	1	1	0	1	1	1	0
6Vdc	1	1	1	0	1	0	1	1
7Vdc	1	1	1	0	1	0	1	0
8Vdc	1	0	1	1	1	1	1	1
9Vdc	1	0	1	1	0	1	1	0
10Vdc	1	0	1	1	1	0	1	1
11Vdc	1	0	1	1	1	0	1	0
12Vdc	1	0	1	0	1	1	1	1
13Vdc	1	0	1	0	1	1	1	1
14Vdc	1	0	1	0	1	0	1	1
15Vdc	1	0	1	0	1	0	1	0

2.2 Packed U-cell Thirty-one-levels

The Packed U-Cell multilevel inverter was proposed the first time by Ounejjar in [8]. This special multilevel inverter is made of one main DC source voltage for one cell and capacitors for the other cells. The configuration

proposed by [8] needs to control the charging and discharging of the capacitors that makes the control very difficult. To overcome this problem and produce more voltage levels, the Packed U cell can be reconfigured like in Fig. 4. This reconfiguration consists to replace the capacitors by the DC sources and use an arrangement that follows 1:3:7:15 ratio. The DC sources are Vdc, 3Vdc, 7Vdc and 15Vdc respectively.



Fig. 4. Packed U-Cell seven-levels (a)[8] and reconfigured thirty-one-levels structure (b).

The switching states of the packed u-cell in thirty-onelevels configuration are depicted in the Table 2. The switches of the same cell operate in a complementary mode by adding an offset of half period. So, if we get the switching states for the positive levels, we use complementary mode by adding an offset T/2 to obtain the switching states for the negative levels. All possible voltage levels are illustrated in Fig. 3.

2.3 Modulation technique

Modulation's techniques are the crucial part for the inverter because it is directly related to the overall efficiency of the entire system [9]. In this part, the modulation technique that applied to control of 31levels inverter is explained. Generally, there are four modulation strategies control of the multilevel inverters such as PWM, Space Vector Modulation (SVM), Duty Cycle Modulation (DCM) [10] and staircase modulation technique [11-17]. The PWM, SVM and DCM techniques are used for the high switching frequency applications that make high power losses. The staircase modulation works on fundamental frequency so all the switches only one time are turned-on and turned off in each cycle. Moreover, if the switching frequency of devices is equal with grid frequency, the power losses are lower than other techniques. In this paper, the staircase modulation called half-height method used and its principle is illustrated in Fig. 5. According to the sine wave, the switching angle is generated when the function value increases to the half height level. The formula for generating the switching angle based on this method is given below.

$$\alpha_i = \sin^{-1}\left(\frac{2i-1}{m-1}\right)$$
, where $i = 1, 2, \dots, \left(\frac{m-1}{2}\right)$ (1)

Output, Voltage (V)

VLoad	S1	S3	S 5	S7	S 9
0	1	1	1	1	1
Vdc	1	1	1	1	1
2Vdc	1	1	1	0	1
3Vdc	1	1	1	1	1
4Vdc	1	1	1	0	1
5Vdc	1	1	1	0	1
6Vdc	1	1	1	0	1
7Vdc	1	1	1	0	1
8Vdc	1	0	1	1	1
9Vdc	1	0	1	1	0
10Vdc	1	0	1	1	1
11Vdc	1	0	1	1	1
12Vdc	1	0	1	0	1
13Vdc	1	0	1	0	1
14Vdc	1	0	1	0	1
15Vdc	1	0	1	0	1

 Table 2. Output voltage levels and switching states for packed u-cell inverter

3 Simulations results and comparative analysis

The PUC multilevel inverter is compared with classical multilevel inverters such as: NPC, FC and cascaded Hbridge inverters based on the asymmetric mode and generation the same voltage levels. The comparison results are presented in Table 3. For the classical inverters and the PUC studied, we considered a singlephase configuration for the comparison. As can see in Table 3, the reconfigured topology in order to generate thirty-one voltage levels at the output requires ten power switches, ten driver circuits and ten Insulated Gate Bipolar Transistors (IGBTs) compared to three other multilevel inverters that require sixteen power switches, sixteen drivers and sixteen IGBTs. The number of DC links of the PUC topology is four that is the same with CHB-MLI and FC-MLI requires six DC links while NPC-MLI requires nine. Spectrum of harmonic of classical CHB and PUC inverters is shown in Fig. 7. Despite we obtain a good spectral content for both the multilevel inverters, percentage of THD of the PUC inverter is given as 2.61 %, which is lower than the classical CHB inverter whose THD value is given as 2.72 %. The obtain THD value contribute to improve the quality of energy which is the main issue in all electrical supply due to various power quality problems. The staircase modulation technique used synthesizing wave forms with better harmonic spectrum and with less THD. This result is confirmed in Fig. 6. in which one can see switching patterns and thirty-one output voltage levels waveform which is similar characteristics with sinusoidal waveform.



Fig. 6. Switching patterns and thirty-one output voltage levels.



Fig. 7. (a) Spectral content of CHB, (b) spectral content of PUC.

Table 3. Parameters comparison between	PUC and classical
inverters	

Parameters	No. Levels	NPC	FC	СНВ	PUC
No. Switches	31	16	16	16	10
No. IGBTs	31	16	16	16	10
No. Drivers	31	16	16	16	10
No. Diodes	31	26	16	16	10
No. DC links	31	9	6	4	4

4 Conclusion

In this paper, a topology of packed u-cell was presented based on reduced switches for grid connected photovoltaic system. The reconfigured structure generated thirty-one levels with a group of four DC sources. In order to reduce the power losses, the proposed modulation technique was half-height staircase modulation, which work in fundamental frequency. For producing all the needed voltage levels, the switching states of IGBTs are determined and depicted in this work. Based on comparison with the classical cascaded H-bridge, the packed u-cell multilevel inverter requires a smaller number of components like switches, drivers, diodes and DC links. For the same voltage levels, PUC has a good value of fundamental and the smallest value of total harmonic distortion which complies with the IEEE 512-2014 standard. For the next future work, the packed u-cell will

be implemented with staircase modulation technique in order to show the performance of the reconfigured PUC proposed in the grid connected PV systems environment and improved it with the famous DCM for the high voltage applications.

References

- H. Khoun jahan, K. Zare, and M. Abapour, 'Verification of a Low Component Nine-Level Cascaded-Transformer Multilevel Inverter in Grid-Tied Mode', *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 1, pp. 429–440, Mar. 2018, doi: 10.1109/JESTPE.2017.2772323.
- [2] V. Sonti, S. Jain, and S. Bhattacharya, 'Analysis of Modulation Strategy for the Minimization of Leakage Current in the PV Grid Connected Cascaded Multi-Level Inverter', *IEEE Trans. Power Electron.*, vol. 32, pp. 1–1, Jan. 2016, doi: 10.1109/TPEL.2016.2550206.
- R. H. Baker and L. H. Bannister, 'Electric power converter', US3867643A, Feb. 18, 1975 Accessed: Jun. 12, 2022. [Online]. Available: https://patents.google.com/patent/US3867643A/ en
- [4] A. Nabae, I. Takahashi, and H. Akagi, 'A New Neutral-Point-Clamped PWM Inverter', *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981, doi: 10.1109/TIA.1981.4503992.
- [5] T. A. Meynard and H. Foch, 'Multi-level conversion: high voltage choppers and voltagesource inverters', in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, Jun. 1992, pp. 397–403 vol.1. doi: 10.1109/PESC.1992.254717.
- [6] K. Srivastav, A. K. Sahoo, K. V. Iyer, and N. Mohan, 'Modulation, control, and performance analysis of asymmetric modular multilevel converter (A-MMC)', *IET Power Electron.*, vol. 11, no. 5, pp. 834–843, 2018, doi: 10.1049/ietpel.2017.0366.
- [7] H. Nademi, A. Das, R. Burgos, and L. E. Norum, 'A New Circuit Performance of Modular Multilevel Inverter Suitable for Photovoltaic Conversion Plants', *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 2, pp. 393–404, Jun. 2016, doi: 10.1109/JESTPE.2015.2509599.
- [8] Y. Ounejjar, K. Al-Haddad, and L.-A. Grégoire, 'Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation', *IEEE Trans. Ind. Electron.*, 2011, doi: 10.1109/TIE.2010.2050412.
- [9] K. El-Naggar and T. H. Abdelhamid, 'Selective harmonic elimination of new family of multilevel inverters using genetic algorithms', *Energy Convers. Manag.*, vol. 49, no. 1, pp. 89–95, Jan. 2008, doi: 10.1016/j.enconman.2007.05.014.
- [10] G. M. Ngaleu, C. H. Kom, A. T. Yeremou, S. Eke, and A. Nanfak, 'Design of New Duty-Cycle Modulator Structures for Industrials Applications, an Alternative to Pulse-Width Modulation', *Eur.*

J. Electr. Eng., vol. 23, no. 2, pp. 103–111, Apr. 2021, doi: 10.18280/ejee.230203.

- [11] S. K. Sahoo and T. Bhattacharya, 'Phase-Shifted Carrier-Based Synchronized Sinusoidal PWM Techniques for a Cascaded H-Bridge Multilevel Inverter', *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 513–524, Jan. 2018, doi: 10.1109/TPEL.2017.2669084.
- [12] H. Yu, B. Chen, W. Yao, and Z. Lu, 'Hybrid Seven-Level Converter Based on T-Type Converter and H-Bridge Cascaded Under SPWM and SVM', *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 689–702, Jan. 2018, doi: 10.1109/TPEL.2017.2664068.
- [13] A. Zhetessov and A. Ruderman, 'Simultaneous Selective Harmonic Elimination and Total Harmonic Distortion minimization for a singlephase multilevel inverter with staircase modulation', May 2017, pp. 729–734. doi: 10.1109/OPTIM.2017.7975055.
- [14] N. Prabaharan and K. Palanisamy, 'Analysis of cascaded H-bridge multilevel inverter configuration with double level circuit', *IET Power Electron.*, vol. 10, no. 9, pp. 1023–1033, 2017, doi: 10.1049/iet-pel.2016.0506.
- [15] K. V. Kumar and R. S. Kumar, 'Switching Sequence Control Of Reduced Switch Count Multilevel Inverter With Multi Carrier Pulse Width Modulation', *Int. J. Sci. Technol. Res.*, vol. 8, no. 12, pp. 3790–3798, Dec. 2019.
- [16] B. McGrath and H. du T. Mouton, 'One-Dimensional Spectral Analysis Techniques for Multilevel PWM Strategies', *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6910–6919, Oct. 2016, doi: 10.1109/TPEL.2015.2511154.
- [17] P. M. Meshram and V. B. Borghate, 'A Simplified Nearest Level Control (NLC) Voltage Balancing Method for Modular Multilevel Converter (MMC)', *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 450–462, Jan. 2015, doi: 10.1109/TPEL.2014.2317705.
- [18] A. R. Kumar, M. S. Bhaskar, U. Subramaniam, D. Almakhles, S. Padmanaban, and J. Bo-Holm Nielsen, 'An Improved Harmonics Mitigation Scheme for a Modular Multilevel Converter', *IEEE Access*, vol. 7, pp. 147244–147255, 2019, doi: 10.1109/ACCESS.2019.2946617.



Fig. 2 All possible output voltage levels for the cascaded H-bridge inverter.



Fig. 3 All possible output voltage levels for the packed u-cell inverter.