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Characteristics investigation on 4.5kV IGBT with partially narrow mesa and split-gate

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Abstract. Low on-state voltage and low turn-off loss are key issues for IGBT used in HVDC and FACTS. Partial narrow mesa was introduced to improve emitter side contact resistance of IGBT based on Nakagawa limit assumption. However, turn-off loss increases and short circuit sustainability get worse. Split gate separates gate electrode from drift region and reduces gate-collector capacitance to lower turn-off energy loss. Combination partial narrow mesa with split gate can get better gate performance and turn-off characteristics in 4.5kV IGBT. Simulated results with TCAD show proposed models improves switching loss and gate reliability. By adjusting split gap electric filed, split gate shape has an important effect on turn-on characteristics.

1 Introduction

High voltage Insulated Gate Bipolar Transitor (IGBT) is emerging key power switching device in HighVoltage Direct Current (HVDC) and Flexible AC Transmission Systems (FACTS). The key technologies of silicon IGBT device focus on the trade-off between breakdown voltages, conductance dissipation and switch energy loss. IGBT reduces on-state voltage drop by increasing injection efficiency of emitter-side. During technology revolutions, most approaches increasing emitter side electron injection efficiency have been adopted to lower on-state voltage drop, such as Wide Gate IGBT proposed by Toshiba in 1993, Carrier Storage Trench IGBT (CSTBT) presented by Mitsubishi in 1996, Narrow Trench with dummy cell (T-IEGT) invented in 1998, Planar IGBT with high conductivity proposed by Hitachi (HiGT) [1], and Enhanced planar IGBT developed by ABB in 2006. All the improved structure have enhanced emitter side electron injection efficiency, and also introduced high conductance modulation in drift region. For silicon IGBTs, the breakdown and on-state voltage drop comply with the characteristic limit rules.

For further improvement for forward characteristic of IGBT, A. Nakagawa proposed the silicon limit theory based on narrow mesa structure in 2006 [2]. That is, when the distance between adjacent gate trenches shrinks to some limit, two channel inversion layers will be close to merging. It sees that only electrons flow through emitter side, and holes only

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donate to conductance modulation. Electron injection efficiency of emitter side is approximately to 1, which achieves an extremely low on state voltage drop. However, it leads to difficult process and worse contact resistance. In order to reduce the influence of the two aspects, a partial narrow MESA (PNM) and a double gate (DB) PNM structure based Nakagawa silicon limit assumption [3-4] were presented to improve contact resistance and to reduce turn-off. Storage carriers increase in PNM lead dv/dt lower and turn-off energy loss larger. A split gate structure was proposed to reduce the gate-drain charge and optimize local electric field in low voltage power MOSFET [5-6], and also were introduce in trench IGBT, CSTBT, and RC-IGBT, to improve the complex tradeoff between switch energy loss, on-state voltage drop, SOA and dv/dt noise[7-11].

In this paper, the split gate structure was introduced in 4500V PNM IGBT to improve turn-off characteristics by lower miller capacitance. The optimized split gate was proposed to further reduce capacitance between gate and collector by modulate the electric field surrounding PNM gate bottom.

2 PNM structure and split gate

2.1 PNM structure

The IGBT proposed by Nakagawa is shown in Fig. 1 (a). If the adjacent mesa width is close to inversion layer thickness, two channel inversion layers in adjacent trench gate, merge into a high concentration n-type layer, which becomes as a hole barrier. If mesa width is less than 40 nm, electron density in the inversion layer will exceed $1.0e^{+17}$ cm^{-3}, and electron injection efficiency can be up to 0.9. Comparison of IGBT characteristic limit among the assumption theoretical calculated, typical Si IGBT and other devices with different materials, is seen in Fig. 1 (b). In the same blocking voltage level, the on-state specific resistance of Nakagawa structure is lower up to one order of magnitude than that of typical Si IGBT, and even better than SiC MOSFET above 2000V.

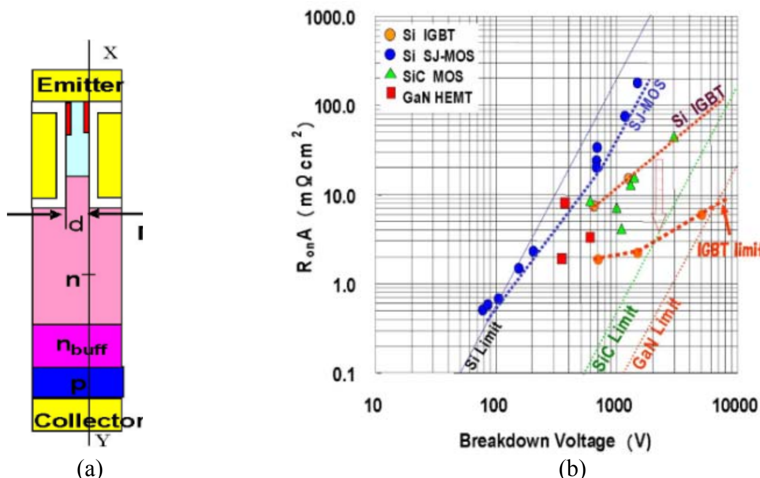


Fig. 1. Nakagawa-limit assumption and characteristic[2] (a) Narrow Mesa, (b) blocking voltage vs. specific resistance.

Although Nakagawa-limit structure can achieve the best on-state characteristic in theory, it results in fabrication process difficulty and the electrode performance deterioration because of high contact impedance. In order to improve it, the PNM structure proposed by M. Sumitomo et al., as shown in Fig. 2 (a), a very narrow mesa is only at the bottom of the

trench. When the distance between the arc regions at the bottom of the adjacent trenches is narrow enough to merge the carrier accumulation layers, behaving as that of Nakagawa-limit structure. The structure can be etched by isotropic method, so the process is greatly simplified. Fig. 2 (b) is the experimental results of different mesa spacing of PNM structure.

The PNM structure takes into account the trade-off between on-state voltage drop and the switching loss. However, due to injection carriers increasing, the storage time becomes longer, thus the dv/dt decreases, and the turn-off energy loss (E_{off}) increases significantly compared with conventional trench IGBT. Although the E_{off} can be reduced by increasing di/dt with a lower collector injection efficiency, it conflicts with the goal of maintaining a low saturation voltage drop.

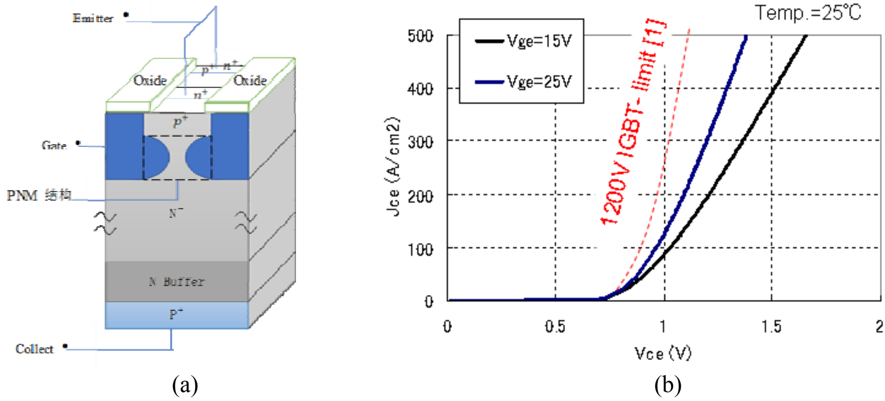


Fig.2. Structure, process and measurement of PNM IGBT [3]: (a) PNM structure, (b) Forward characteristics between PNM measured and Nakagawa-limit calculated (at mesa wide=30nm, 1200V).

2.2 Split gate

For further lower switching loss, the Miller capacitance has to be reduced to increase dv/dt during switching. However, more trench gate area causes large Miller capacitance. Split Gate[5-9], originally proposed in MOSFET, is a reasonable structure which can realizes high injection effect and low Miller capacitance. Schematic cross sectional views of split gate in Vertical Double-diffused MOSFET (VDMOS) and IGBT, is seen as Fig.3.

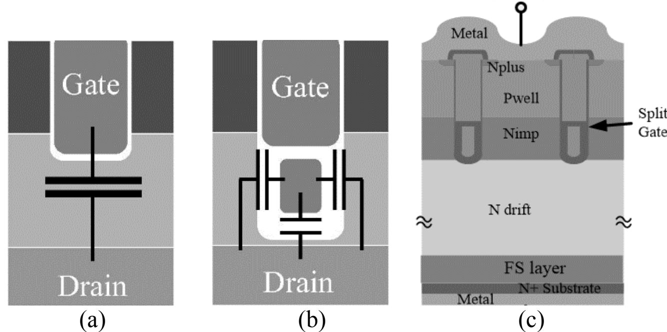
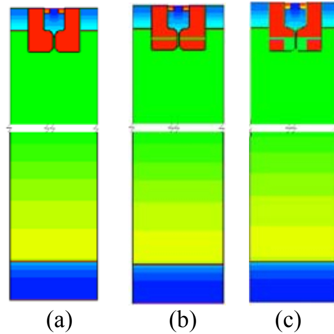


Fig. 3. Schematic cross-sectional views of (a) conventional trench gate, (b) split gate, and (c) split-gate IGBT.

The breakdown voltage in the above references is between 600V and 1200V. Although the analytical calculation results and TCAD simulation results of 4.5kV devices based on Nakagawa-limit are also given in reference [2], there is a larger deviation.



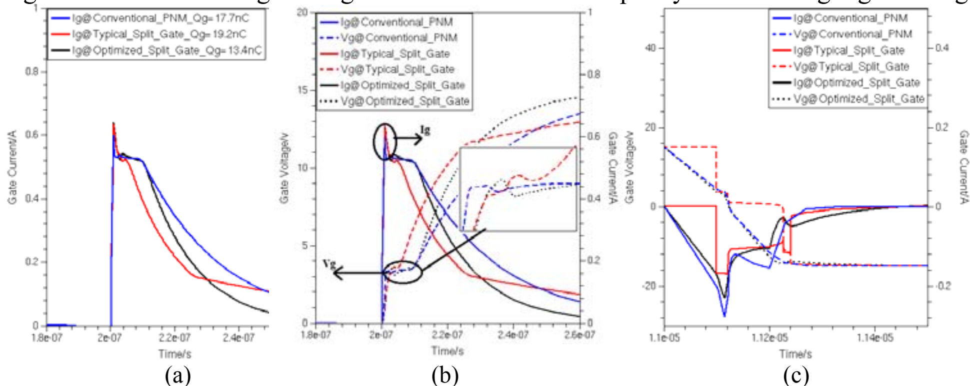
(a) (b) (c)

Fig. 4. The proposed different 4.5kV PNM-IGBTs with (a) conventional PNM, (b) typical split-gate PNM, and (c) optimized split-gate PNM.

In order to obtain a better device structure close to Nakagawa-limit in 4500V voltage level, in this papers, an improved PNM-IGBT model was established, as shown in Fig. 4 (a). For lower gate-collector capacitance, the split-gate(SG) is introduced into the PNM trench, as shown in Fig. 4 (b). For further improved to dv/dt, an optimized split-gate is proposed in Fig.4(c), which has smaller trench gate area face to collector. Lower miller capacitance will achieve high dv/dt and turn-of energy loss.

3 Simulation and discussion

The gate characteristics of proposed different structures simulated by TCAD are shown in Fig.5. It can be seen that the optimized split-gate (OPSG) has the smallest total gate charge during turn-on, being up to 13.4nC. It attributes to the lateral trench polysilicon being replaced by oxide, which attains a lower capacitance between gate and collector. Generally, split-gate can reduce gate-collector capacitance and gate charges during turn-on, but the gate charge of typical split-gate (TPSG) is slightly larger than conventional PNM (CPNM). Higher tail current during turning on and shorter miller step may induce to lager gate charge.



(a) (b) (c)

Fig. 5. Gate characteristics comparison among the proposed structures, (a) gate current during turn-on, (b) miller voltages during turn-on, (c) gate current and voltage during turn-off.

3.1 Miller Plateau and gate turn-on characteristics

Fig.5(b) show the gate current peak and gate voltage changes in the Miller Plateau of the presented models. From the inset in Fig.5(b), the Miller Plateau of TPSG structure is the shortest, while the width of Miller platform of CPNM and OPSG is close to. In OPSG it

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transit slowly to Miller Plateau, and the voltage increment is more than that of CPNM. The gate current peak of TPSG is the largest, but the gate miller current is very short. The gate miller current of CPNM is close to that of OPSG. When transited by Miller Plateau, gate current of CPNM is the largest, and OPSG is the smallest. During tail stage, the TPSG current increases and the TPSG voltage decreases.

The results show that uniform electric field and charge distribution at the bottom of narrow mesa is very important to Miller Plateau, and miller width will affect turn-on characteristics.

The gate current and voltage curves during turning off are shown in Fig.5(c), in which TPSG has sharply step changed characteristics, and OPSG or CPNM has gradually changed performance. These results will be the causes of following turn-off characteristics.

3.2 Split-gate and switching power loss

Switching characteristics comparison between the presented IGBTs is shown in Fig.6. During turn-on, CPNM and OPSG have similar collector voltage and current, which attributes to have same Miller Plateau as Fig.5(b). Due to extremely narrow Miller platform, TPSG IGBT can't turn on quickly and will result larger power loss.

During turning off, TPSG and OPSG have similar characteristics, and CPNM has longer storage charge extraction and total turn-off time. Therefore, split-gate can reduce the gate collector capacitance and cut down total turn-off time, furthermore lower turn-off loss.

There are some rugged oscillations in TPSG turn-off curves, which is related to the abrupt change of gate capacitance caused by shield oxide gap in Fig.5(c). The gate voltage and current abrupt changes in TPSG lead to irregular swings of turn-off collector current and voltage. Due to the thicker oxide in OPSG shielding gate inducing uniform charge distribution, the gate current and voltage change continually. For variation of gate voltage and current of OPSG is similar to CPNM, their turn off characteristics are little deviation.

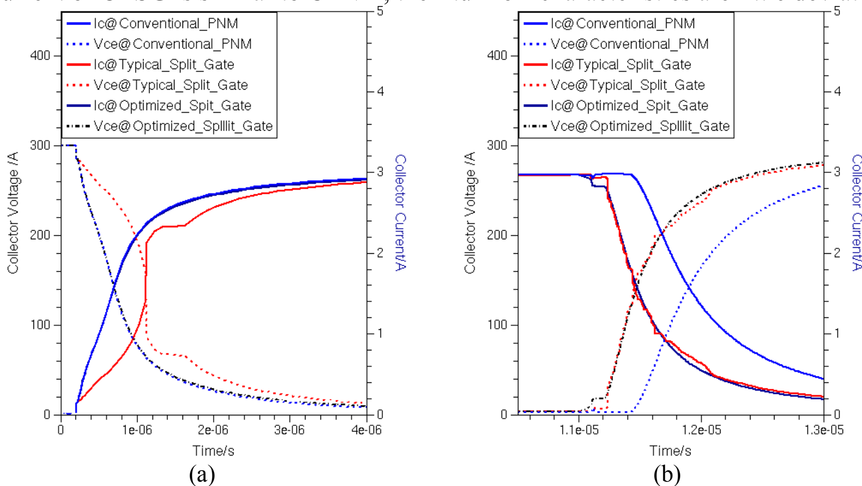

Fig. 6. Comparison of collector current and voltage, (a) during turn-on, (b) during turn-off.

By above analysis, it can be concluded that the gate shape influence on turn-off characteristics of PNM IGBT is closely related to the profile continuity of charge and electric field in the narrow mesa bottom.

4 Conclusion

The PNM structure and the implemented technology presented by references solve the characteristic influence and process difficulty caused by Nakagawa's very narrow mesa. A new partial narrow mesa, split-gate and optimized split-gate structures are introduced improve characteristic limit of 4.5kV IGBT. The gate miller and switching characteristics of three proposed structures are compared and simulated. TCAD results show, that optimized split-gate IGBT has similar Miller Plateau and turn-on curves with the conventional PNM IGBT, and has more reliability turn-off characteristics than presented typical split-gate IGBT. Split-gate shape has an important influence on turn-on characteristics by changing Miller Plateau. Split-gate lowers turn-off loss by reducing gate collector capacitance and cutting down total turn-off time. Moreover, adjusting the shape of split-gate will further improve switching power loss of IGBT.

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