

Design of domestic serial and parallel interface module

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Abstract. Domestic serial and parallel interface module is based on domestic high performance FPGA CPCIE module. This type of FPGA has rich logical resources and internal integration of a variety of high-speed interfaces, such as PCIE, high-speed Serdes interface, which can achieve serial port, time system, network and other interfaces design, greatly simplifying the hardware design of the module. The main communication interfaces, PCIE and UART, are realized by the IP core of FPGA, realizing the integration of the main functions on the chip, which greatly improves the flexibility and expansibility of the design.

1 Introduction

Serial communication has been widely used because of its few transmission lines, low cost and flexible configuration. Universal Asynchronous Receiver/Transmitter is a common interface circuit, which is mainly used for the conversion of serial data and parallel data. Generally, the interface is completed by a special UART chip, such as sc16c554bib64. The interface chip has four independent channels and provides a variety of control functions at the same time. However, in practical use, only one specific control mode is often used, which not only causes the circuit complexity and waste, but also increases the PCB area and wiring complexity.[1]

FPGA, field programmable gate array, is a kind of semi custom circuit in the field of application specific integrated circuit. It not only solves the shortcomings of custom circuit, but also overcomes the shortcomings of limited gate circuits of original programmable devices. FPGA has rich flip flops and I / O Interface, Using description language (VHDL and Verilog HDL) to design, users can describe the circuit with various functions according to their needs[2].

With the improvement of localization requirements of various services, products based on Loongson and Shenwei processor platforms are becoming more and

more popular. Under the background of independent control, this design proposes a design scheme of CPEX reinforced serial port module based on domestic FPGA.

The main communication interfaces of domestic serial and parallel interface module, such as PCIE and UART, are implemented with the IP core of FPGA. The main functions are integrated on chip, which greatly improves the flexibility and scalability of the design.

2 Key technology

Domestic serial and parallel interface module, takes the lead in the research and development of single board reinforcement module with CPEX architecture for naval equipment. FPGA peripheral configuration power supply and flash loading are all domestic chips.

The main communication interfaces of the Domestic serial and parallel interface module, such as PCIE and UART, are implemented with the IP core of FPGA. The main functions are integrated on chip, which greatly improves the flexibility and scalability of the design.

3 Hardware design

The block diagram of hardware design principle is shown in Figure 1.

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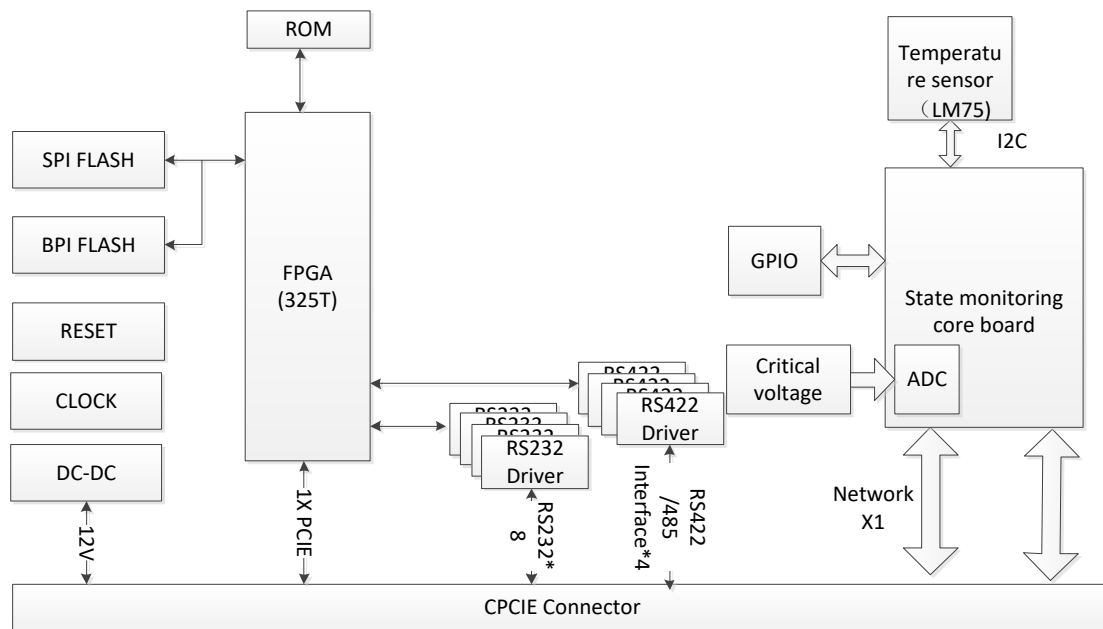


Fig. 1. Block diagram of hardware design principle.

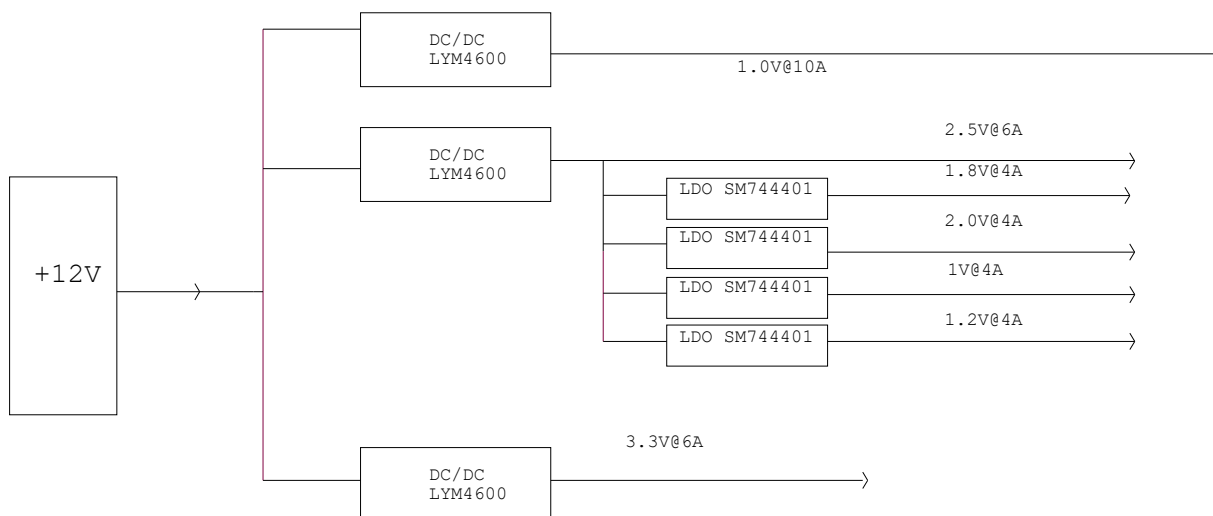


Fig. 2. Power block diagram.

3.1 Design of power supply circuit

The whole board voltage of the module is +12V and +5V from the CPEX connector_ BMC, where +5V_ BM voltage is specially used to supply power to the management module of the module, and other voltages required by the module are converted from +12V voltage through the power chip. The specific power supply design is shown in Figure 2.

3.2 Design of 8-way isolated RS232 interface

In order to improve the generality of the module, 8-Channel RS232 is designed with separate isolation for each channel, and ADI's adm3252 is used as the transceiver. The transceiver mainly has the following characteristics:

a) The internal level is 3.3V, which can be directly connected with FPGA;

- b) Internal integrated isolation power supply, improve the integration, simplify the design and reduce the board pair;
- c) The speed can reach 460kbps;
- d) Isolation voltage 2500V.

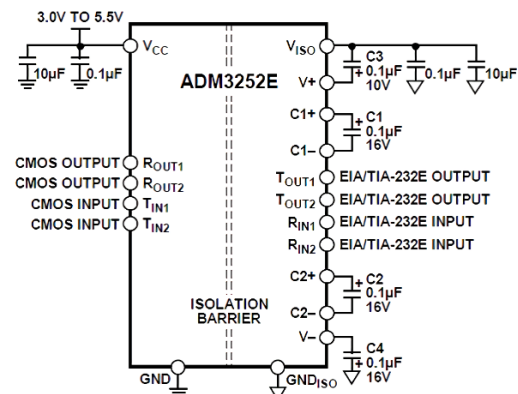


Fig. 3. ADM3252 Typical application circuit.

3.3 Design of 8-channel isolated RS485 / 422 interface

The transceiver adopts adm2582 of ADI company, which mainly has the following characteristics:

- The internal level is 3.3V, which can be directly connected with FPGA;
- Internal integrated isolation power supply, improve the integration, simplify the design and reduce the board pair;
- The speed can reach 16mbps;
- Isolation voltage 2500V.

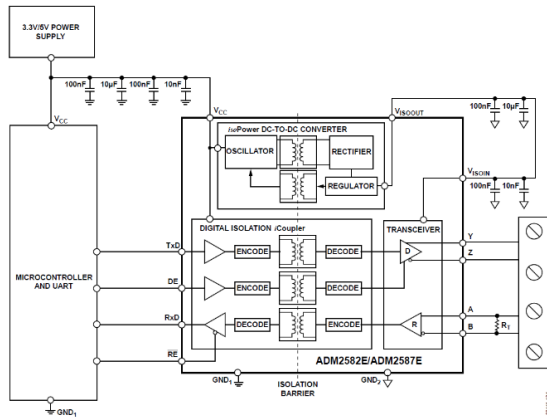


Fig. 4. ADM2582 Typical application circuit.

3.4 Design of RS232 / 422 / 485 interface protection circuit

RS232 external interface is single ended input and output, the input voltage range is $\pm 30V$, and the output voltage is $\pm 5V$. The input and output interfaces protect the isolated grounding TVs tube of 20V / 5A to prevent the interface chip from being damaged due to the common ground problem in harsh environment.

RS422 / 485 external interface is differential input and output, standard RS422 level, in order to prevent the input voltage from logic 1 when the external interface is disconnected, the up and down processing is carried out on the input and output interfaces. The input and output interfaces protect the isolated ground connected 5V / 5A TVS tube to prevent the interface chip from being damaged due to the common ground problem in harsh environment. RS422 / 485 interface is equipped with 120 ohm short-circuit resistor, which can be selected by winding.

3.5 RS232/422 /485 interface switching design

Each RS232/RS422/RS485 interface shares one UART IP core, which is controlled by FPGA. RS422 is compatible with RS485 interface level, so RS422/RS485 interface share one interface chip, RS485 uses RS422 interface TX+ and TX- signal definition. The RS232 interface level is not compatible with RS422, so another RS232 interface chip is used. The RS232 / 422 / 485 interface configuration adopts the wire winding mode. The signal of the interface chip is connected to the CPCIE connector through the wire winding to realize the interface configuration. At the same time, a group of IO signals represent the configuration of

the interface. FPGA reads the configuration information of the interface mode, and the host computer reads the interface configuration mode in FPGA to realize the configuration of the interface driver and display it in the host computer.

3.6 RS232/422 /485 interface switching design

The 16 channel universal I/O interface is designed in the board, which has no interrupt mode. The interface chip adopts sm74alvc164245pvg8, the input and output level is $\pm 5V$, and the interface current driving capacity is $\pm 24mA$.

3.7 BMC management extension design

- The Domestic serial and parallel interface module contains independent IPMI to collect the temperature and other information of each key circuit core of FPGA on the board. Through the judgment of the above information, it determines whether each voltage circuit is faulty. At the same time, it determines whether the temperature of each part of the circuit is normal through the judgment between the real-time temperature measurement value and the preset threshold value. Finally, it provides the relevant measurement information through the man-machine interface, which is necessary Alarm information is provided when the system is running. The principle of IPMI environment information collection is shown in Figure 6.

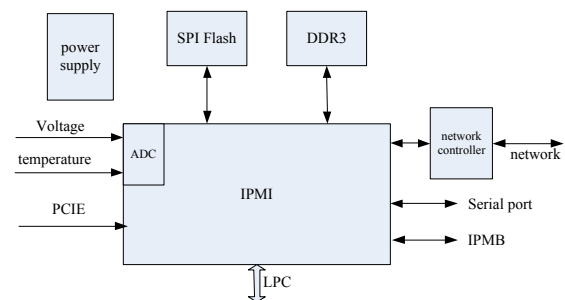


Fig. 5. IPMI principle block diagram

- The serial and parallel interface expansion module supports the software self-test function, and the fault can be located at the module level when the self-test error is reported.
- All the necessary test points are led to the interface. When the system fails, the software self-test and test equipment detection are used for fault detection, so as to improve the correctness of fault location and reduce the fault location time.
- Each module in the module serial and parallel interface expansion module can use various test fixtures, such as the test board, to build a complete test environment independent of the chassis, to test the function of each module, to provide verification of various interfaces and performance indicators, and to determine whether each module can work normally.

4 Conclusion

In recent years, the products of domestic processors are more and more widely used in the field of weapons and equipment. Based on the background of self-control and project requirements, the design scheme of CPEX reinforced serial port module based on jfm7k325t-fcbga90 is proposed, and the main hardware architecture is nationalized, It not only ensures the function of the product, but also has the same performance as other foreign platform products that have been equipped, and has a wide range of application scenarios.

References

1. Yingqiang YANG.(2005)Realization of a Sort of UART Based on FPGA [J].Modern Electronics Technique.
2. WANG Jie,WANG Cheng,XIE Long-han. (2011)Xilinx FPGA/CPLD Design Manual[M].Posts & Telecom Press..
3. Li Wei. (2015) Design and implementation of multi serial communication based on FPGA. Digital technology and Application,174~177.
4. Zhang gui,Qianqian Ma,Peiyuan Gong. (2017) Design of universal serial interface circuit based on FPGA. Communication design and Application, 88~89.